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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/533,550	11/17/2005	Andrew Graham	1432.116.101/P29858	6310

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EXAMINER	
LE, THAO P	

ART UNIT	PAPER NUMBER
2818	

MAIL DATE	DELIVERY MODE
05/21/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/533,550	GRAHAM ET AL.	
	Examiner	Art Unit	
	THAO P. LE	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 March 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *22-25,27-37 and 39-45* is/are pending in the application.

4a) Of the above claim(s) *43 and 45* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *22-25, 27-37, 39-42, 44* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *4/29/05* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This office action is in response to amendment and argument filed on 03/18/2009.

Claims 1-21, 26, 38 have been cancelled.

Claims 22, 41, 44 are amended.

Claims 43, 45 have been withdrawn.

Claims 22-25, 27-37, 39-42, and 44 are pending.

Remarks of applicant are fully considered but not found persuasive. The newly added limitation of "grown up in a via hole from the bottom of the via hole" is considered as "process of making" while the claims are considered as produce by process.

From MPEP, A "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17(footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Fessmann, 180 USPQ 324; In re Avery, 186 USPQ 161; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); In re Marosi et al, 218 USPQ 289; and particularly In re Thorpe, 227 USPQ 964, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that applicant has the burden of proof in such cases, as the above caselaw makes clear.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 22, 27, 28, 33, 35, 40-41, 44 are rejected under 35 U.S.C. 102(e) as being anticipated by Farnworth et al., U.S. Patent No. 6,515,325.

Regarding claims 22, 27, 41, 44, Farnworth discloses a vertical integrated field-effect transistor comprising (See Fig. 5):

a first electrically conductive layer 77 (Fig. 5);

a middle layer (layers between the layers 77 and 83) formed partially from dielectric material on the first electrically conductive layer 77;

a second electrically conductive layer 83 on the middle layer, and

a nanostructure in the via hole 22, the nanostructure further comprising a first end portion that is coupled to the first electrically conductive layer 77 and a second end portion that is coupled to the second electrically conductive layer 83;

wherein the first end portion of the nanostructure forms a first source/drain region (layer 77 functions as source; Col. 7, lines 32-35) and the second end portion of the nanostructure forms a second source/drain region (layer 83 functions as drain; Col. 7, lines 32-35) of the FET;

wherein the middle layer 81, between two adjacent dielectric sublayers (portions of insulating layer formed below and above layer 81) has a third electrically conductive layer 81, the thickness of the third conductive layer 81 is less than the thickness of at least one of the dielectric sublayers (the thickness of layer 81 is less than the thickness of insulating layer formed on top of layer 81 and below layer 83);

wherein a ring structure formed an electrically insulating material as gate-insulating region of the FET is arranged in the third electrically conductive layer, which forms the gate electrode of the FET, along the via hole that has been introduced therein (the inner portions of the insulating material formed between layer 81 and nanostructure 22).

Still regarding claims 27, 44, Farnworth discloses wherein the middle layer has an additional electrically conductive layer 79/74 which serves as an additional gate electrode of the FET, with an additional ring formed from an electrically insulating material as an additional gate insulating region of the FET being arranged along the via hole that has been introduced in the additional electrically conductive layer (the inner portions of insulating layer that formed between the layer 22 and 79/74).

Still regarding claims 22, 41, and 44, the limitation of "a nanostructure grown up in a via hole from the bottom of the via hole" is not considered since it's the product by process limitation. The patentability of a product does not depend on its method of production. See MPEP 2113.

Regarding claim 28, Farnworth discloses the FET of claim 22 having an additional FET above the FET (Col. 1, lines 60-65).

Regarding claims 33, 35, Farnworth discloses the use of a carbon nanotube as the nanostructure (Col. 2, line 36).

Regarding claim 40, Farnworth discloses a substrate in FET is made of polycrystalline (Col. 4lines 25-27).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 29 is rejected under 35 U.S.C. 103(a) as being unpatentable over Farnworth et al., U.S. Patent No. 6,515,325, in view of Fitch et al., U.S. Patent No. 5,612,563.

Regarding claim 29, Farnworth discloses these FETs are connected to one another and the stack gate is logic gates/circuits but fails to disclose the device is an inverter circuit/gate. Fitch discloses the device is an inverter gate (Figs. 11-12). It would have been obvious to one having ordinary skill in the art at the time the invention was made to have the device in Farnworth is a inverter gate as of Fitch's because the device in Farnworth is a logic gates and the inverter conventionally is a logic gate, and the device in Farnworth is formed as an inverter gate as in Fitch's would reduce the processing cost.

Claims 30-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Farnworth et al., U.S. Patent No. 6,515,325, in view of Watanabe et al., U.S. Publication No. 2002/0130333.

Regarding claims 30, 31 Farnworth fails to disclose the first, second, third, and additional electrically conductive layers include one of a group comprising tantalum, TaN, Ti, Mo, Al, TiN, and a ferromagnetic material. Watanabe discloses the first, second, third and additional electrically conductive layers include Ti [0053]. It would have been obvious to one having ordinary skill in the art at the time the invention was made to use Ti material as first, second, third, and additional conductive layers as in Watanabe in the structure of Farnworth because Ti material provides high conductivity.

Claims 23-25, 36, 42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Farnworth et al., U.S. Patent No. 6,515,325, in view Mancevski, U.S. Publication No. 2001/0023986.

Regarding claim 23, Farnworth fails to disclose the use of catalyst material for catalyzing the formation of the nanostructure is arranged between the first conductive layer and the nanostructure. Mancevski discloses the use of catalyst material for catalyzing the formation of the nanotube is arranged between the first conductive layer and the nanotube ([0013], [0041]; the catalyst 54 is deposit in the inner walls and on the bottom of the via hole 50). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the nanotube of Farnworth by

having catalyst material for catalyzing the formation of the nanotube starting from the bottom of the via hole as disclosed in Mancevski because catalyst is used at the bottom of the nanotube will provide aligned nanotube within a catalyst retaining template and the growing of nanotube material can be controllable.

Regarding claim 24, Farnworth discloses the third electrically conductive layer 81 surrounds the nanostructure in a region around the first end portion (See Fig. 5).

Regarding claims 25, 42, Farnworth fails to disclose the thickness of the third electrically conductive layer is less than the thickness of both dielectric sublayers. Mancevski discloses wherein the thickness of the third conductive layer is less than the thicknesses of both dielectric sublayers (the thickness of the third conductive layer is where the growth of nanostructure is discontinued, Figs. 1-4). It would have been obvious to one having ordinary skill in the art at the time the invention was made to have the thickness of the third conductive layer is less because the thicknesses of the sublayers more than the thickness of the third conductive layer would provide reduction in parasitic capacitance in the device and to improve thermal distribution from the active cells thereby reducing the likelihood of thermal damage to the device.

Regarding claim 36, Farnworth fails to disclose the use of catalyst and wherein the catalyst material is one of a group comprising iron, cobalt, and nickel. Mancevski discloses wherein the catalyst material is one of a group comprising iron, cobalt, and nickel. It would have been obvious to one having ordinary skill in the art at the time the invention was made to use iron, cobalt, and nickel as catalyst because iron, cobalt, and nickel catalysts have better diffusion and the rate of nanostructure's growth is faster.

Claims 32, 39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Farnworth et al., U.S. Patent No. 6,515,325.

Regarding claim 32, Farnworth discloses the middle layer (isolation layer 20) is any insulating material but fails to disclose the middle layer is SiO or SiNi. It is well known in the art that the insulating material such as SiO or SiNi is widely used as dielectric material because SiO or SiNi provides better insulation which separates the first, second, and third electrically conductive layers from one another.

Regarding claim 39, Farnworth discloses the FET of claim 22 formed exclusively from dielectric material, conductive material, and the material of the nanostructure but fails to disclose the conductive material is metallic material. It is well known in the art that metallic material is widely used as conductive material because metallic material provides high conductivity.

Claim 34 is rejected under 35 U.S.C. 103(a) as being unpatentable over Farnworth et al., U.S. Patent No. 6,515,325, in view of Banin et al., U.S. Publication No. 2003/0214699.

Regarding claim 34, Farnworth fails to disclose the nanostructure is a nanorod includes one of a group comprising silicon, germanium, indium phosphide, gallium nitride, gallium arsenide, zirconium oxide, and a metal. Banin discloses the nanostructure is a nanorod comprises gallium arsenide [0080]. It would have been obvious to one having ordinary skill in the art at the time the invention was made to

have nanorod comprises GaAs because nanorod comprises GaAs would provide the growth of nanostructure conformably and selectively.

Claim 37 is rejected under 35 U.S.C. 103(a) as being unpatentable over Farnworth et al., U.S. Patent No. 6,515,325, in view Mancevski, U.S. Publication No. 2001/0023986, and further in view of Banin et al., U.S. Publication No. 2003/0214699.

Regarding claim 37, Farnworth and Mancevski fail to disclose wherein the nanostructure is a GaAs nanorod and wherein the catalyst material includes gold. Banin discloses the nanostructure is a GaAs nanorod and wherein the catalyst material includes gold [0029-0036, 0080]. It would have been obvious to one having ordinary skill in the art at the time the invention was made to have nanostructure is a GaAs nanorod and wherein the catalyst material includes gold in order to monitor properties of the nanostructure, control the arrangement, density, length of the nanorod, and obtain the growth of the nanostructure selectively.

When responding to the office action, Applicants' are advice to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist the examiner to locate the appropriate paragraphs.

A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the day of this letter. Failure to respond within the period for response will cause the application to become abandoned (see M.P.E.P 710.02(b)).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thao P. Le whose telephone number is 571-272-1785. The examiner can normally be reached on M-T (7-6).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Steven H. Loke can be reached on 571-272-1657. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Thao Le/

Thao P. Le

Primary Examiner

AU 2818